Amendment to the Specification:

Please replace paragraph [0027] with the following amended paragraph:

[0027] Fig. 1 illustrates a basic NAND array architecture implemented with TROM cells according to the present invention. As shown in Fig. 1, the TROM NAND array comprises a plurality of memory cells configured in columns and rows. The columns comprise sets of memory cells that are arranged in series, and which have select transistors on one or both ends of the set for coupling the set of memory cells to bit lines. Thus, as shown in Fig. 1, a first bit line BL1 is coupled via a top select transistor 13 to a set of memory cells 12-1, 12-2, ... 12-n connected in series. At the opposite end of the set of memory cells, a select transistor 14 is provided. The select transistors 13, 14 are responsive to decoded block select signals SEL-T at the top of the set, and SEL-B at the bottom of the set. The select transistor 13 typically connects directly to the bit line BL1, while the select transistor 14 may connect to a ground reference coupled to bias line 21 or to an adjacent bit line, depending on the decoding arrangement for the bit lines. Word lines WL1, WL2, ..., WLn are coupled to the gates of memory cells along respective rows in the array.

Please replace paragraph [0031] with the following amended paragraph:

[0031] Fig. 3A is a cross-sectional view taken on a line from channel terminal 60 to channel terminal 61 across the word line 56 of Fig. 2. The semiconductor substrate 80 includes a deep n-type well 81. The semiconductor bulk for the memory cell is formed in the isolated p-type well 82. Diffusion regions 60 and 61 are spaced apart with channel region 84 therebetween. The multilayer film overlying the channel region 84 includes a bottom oxide 85, a trap ~~player~~ layer 86, and a top oxide 87. Word line 56 overlies the multilayer film acting as a gate for the cell. As result, a memory cell with a first channel terminal 60, a second channel terminal 61, and a channel 84 therebetween is provided with a charge trapping structure (trap ~~player~~ layer 86) between the channel 84 and the gate 56. The isolated p-type well is doped in embodiments of the present invention, so that the cell threshold with neutral charge in the charge trapping layer is

slightly negative. In this manner, the channels in the memory cells are normally conductive reducing the impedance of the series connected set of memory cells and improving performance.

Please replace paragraph **[0033]** with the following amended paragraph:

[0033] Fig. 3B is a cross-sectional view taken on a line from STI structure 51 along the word line 56 to the STI structure 52 of Fig. 2. Structures shown in Fig. 3A are given the same reference numerals as Fig. 3B. Fig. 3B shows the isolation provided by the STI structures 51, 52 between the channel regions (e.g. [[89]] 84) of the memory cells. Also, the multilayer film including bottom oxide 85, trap ~~player~~ layer 86, and top oxide 87 extends along the line under the word line 56 in this embodiment. In other embodiments, the multilayer film may be limited to patches over the channel regions of the memory cells.

Please replace paragraph **[0034]** with the following amended paragraph:

[0034] The charge trapping structure (trap ~~player~~ layer 86) comprises a continuous layer of silicon nitride across the channel region in the illustrated example. In other embodiments, the charge trapping structure may comprise one or more isolated pockets of charge trapping material. Also, charge trapping materials other than silicon nitride may be utilized, including for example metal oxides such as HfOx, ZrOx, AlOx and others.

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